

IN THE CLAIMS:

1. (Currently Amended) A deblocking filter arithmetic apparatus comprising:

a ~~first to an eighth arithmetic blocks which receive~~ respectively, each for receiving, as inputs, simultaneously every two adjacent pixel data among a first to an eighth pixel data, ~~carry for carrying out in parallel one of the cycles of~~ the ~~processing arithmetic constituting the processing comprising~~ filter filtering processing corresponding to of first to eighth pixel data and ~~performed for removal of removing~~ block noises, every time when two of the pixel data are input, and output the each for outputting respective filtered pixel data having been subjected to the filtering processing, being provided in parallel and corresponding to the first to the eighth pixel data and to which two of the pixel data are input simultaneously;

an output selection circuit ~~which selects for selecting one~~ from the of outputs from the first to the eighth arithmetic blocks and ~~outputs for outputting~~ the same; and

a control circuit ~~which controls for controlling~~ the ~~processing arithmetic~~ processing of each arithmetic block, in

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accordance with the cycles of the ~~pre~~processing—arithmetic processing, so that:

the cycles of the ~~pre~~processing—arithmetic processing
performed in on each combination of arithmetic blocks up to the
conclusion of the filter processing should be the same, among a
combination of the a first and the second arithmetic block, a
combination of the a third and the fourth arithmetic block, a
combination of the a fifth and the sixth arithmetic block, and a
combination of the a seventh and the eighth arithmetic block,
respectively, ~~constituted by above-described arithmetic blocks~~
~~up to the conclusion of the respective filtering processing~~
~~should be the same and, further~~

so that the filtering filter processing of each combination
of arithmetic blocks is ~~should be concluded in an order~~
successively among the respective combinations, and which
~~controls the~~

said control circuit also for controlling said output
selection circuit ~~so as to select the output from the arithmetic~~
blocks in a ~~unit of the~~ for each combination of the arithmetic
blocks and to perform a pipeline output.

2. (Currently Amended) A ~~The~~ deblocking filter arithmetic apparatus ~~as defined in of~~ claim 1 wherein, the arithmetic block comprises:

a first selection circuit which ~~selects~~ for selecting, according to the ~~a~~ cycle of the ~~processing~~ arithmetic processing, ~~any one among one either~~ of two simultaneously inputted pixel data ~~input simultaneously~~, two values obtained respectively from the first pixel data and the eighth pixel data, and pixel data which are ~~define~~ adjacent at pixels and correspond to an area outside areas corresponding to the first pixel data and the eighth pixel data respectively, and value 0,

a second selection circuit which ~~selects~~, for selecting, according to the cycle of the ~~processing~~ arithmetic processing, ~~any one among the other of~~ such two simultaneously inputted pixel data ~~input simultaneously~~, two values obtained respectively from the first pixel data and the eighth pixel data, and pixel data which are ~~define~~ adjacent at pixels and correspond to an area outside areas corresponding to the first pixel data and the eighth pixel data respectively, and value 0,

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a third selection circuit ~~which selects~~ for selecting an arithmetic result for the accumulation or value 8,

a first shifter ~~which receives,~~ for receiving, as input, the output of the first selection circuit,

a second shifter ~~which receives,~~ for receiving, as input, the output of the second selection circuit,

an adder ~~which adds~~ for adding together the output of the first shifter, the output of the second shifter and the output of the third selection circuit,

a register ~~which receives,~~ for receiving, as input, the output of the adder and ~~outputs~~ for outputting the ~~same~~ output of the adder as an arithmetic result for ~~the~~ accumulation to the third selection circuit, and

a third shifter ~~which receives,~~ for receiving, as input, ~~the~~ output of the register and ~~outputs~~ for outputting the ~~same~~ output of the register as an arithmetic result to the output selection circuit.

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3. (Currently Amended) A deblocking filter arithmetic method comprising:

~~a step for receiving, as inputs, simultaneously every two data among a first to an eighth successive pixel data and carrying out in parallel the processing arithmetic processing constituting the comprising filter filtering processing corresponding to of the first to the eighth pixel data and performed for removal of removing block noises, so that:~~

~~the cycles of the processing arithmetic processing performed in on each combination of arithmetic blocks up to the conclusion of the filter processing should be the same, among a combination of the a first and the second arithmetic block, a combination of the a third and the fourth arithmetic block, a combination of the a fifth and the sixth arithmetic block, and a combination of the a seventh and the eighth arithmetic block, respectively, constituted by above-described arithmetic blocks up to the conclusion of the respective filtering processing should be the same and, further that~~

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so that the filtering processing of respective combinations
of the pixel data is ~~should be concluded in an order~~
~~successively,~~successively; and

~~a step for performing a pipeline output of pixel data which~~
~~are obtained by the above-described step with having been said~~
receiving and ~~subjected to the filtering filter processing,~~ for
the respective combinations of the pixel data in ~~an order~~
~~successively~~succession.